First Partial Exam Digital Systems A (EE1D1)
4 October 2024, 09.00 – 11.00 h

This exam is an **open book** exam. During the exam you may use: the course book (or any other book about the topic, also prints of books are allowed), the lecture slides, and the lab manual.
NOT allowed are the instruction slides, old tests and exams, notes, and electronic equipment - other than a simple, non-programmable, calculator. If you do not adhere to this, the exam fraud rules apply.

The exam consists of 6 pages and contains **18 multiple choice (MC) questions**, each with equal weight. The MC questions must be answered on the issued MC form. Some instructions when filling in the MC form:

- Only one answer is the correct answer.
- **Draw a cross on the bubble with the letter of your** choice (preferably with ballpoint pen, or with pencil), as shown in the example on the MC form.
- Only fill in the form at the end of the exam to avoid mistakes.
- You may fill a bubble completely to correct your previous answer (see example on the MC form), but if you make more mistakes, it is better to ask for a new MC form.
- Leaving a question unanswered always works to your disadvantage.
- Do not forget to fill out your name and student number (digits and bubbles!).

Good luck!

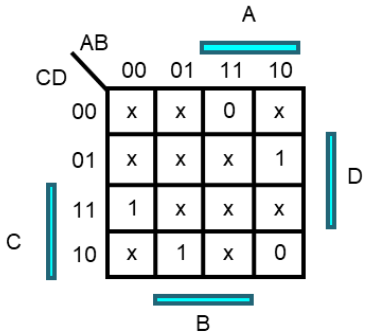
Question 1

What is a valid equivalent expression for Y = (AB + BC')'

a. Y = (A + B)(A' + C')
b. Y = (A' + B')(B' + C)
c. Y = (A + B')(A + C')
d. Y = (A' + B)(A' + C')

Question 2

Given the following K-map. Which of the following statements is true:



a. The number of sum terms in the minimal product-of-sums equals the number of product terms in the minimal sum-of-products
b. The number of sum terms in the minimal product-of-sums is larger than the number of product terms in the minimal sum-of-products
c. The number of sum terms in the minimal product-of-sums is smaller than the number of product terms in the minimal sum-of-products
d. None of the above statements is true

Question 3

How can we represent the value -25 with a floating point number?

- **a.** 1 10000011 10010000000000000000000
- **b.** 1 10000011 10111000000000000000000
- **c.** 1 01111111 10010000000000000000000
- **d.** 0 00000100 10111000000000000000000

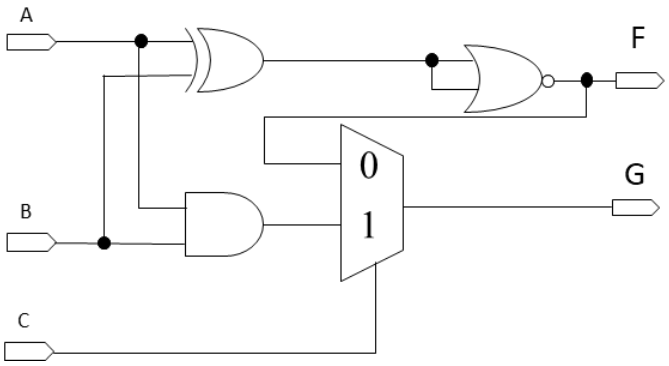
Question 4

Two numbers A = 000101 and B = 101011, in 2's complement notation, are subtracted as follows: B-A. What is the outcome of this operation in 2's complement notation?

a. 000110 **b.** 010000 **c.** 110000 **d.** 100110

Question 5

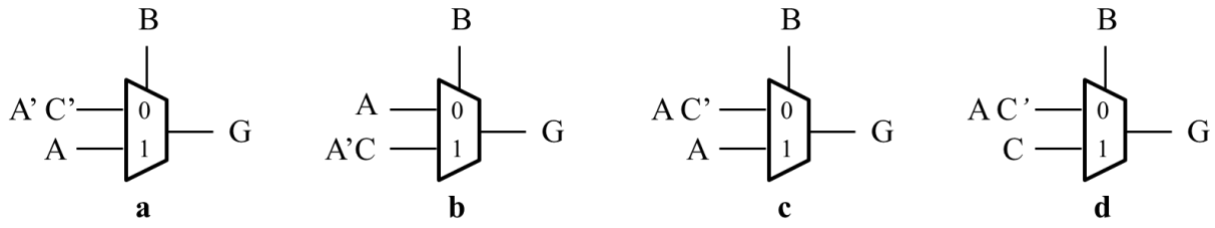
Given the circuit at the right. The delay time for a AND gate is 5 ps, for a NOR gate 5 ps, for an EXOR gate 8 ps, and for a MUX 2 ps (from any input to the output). Initially, just before t = 0 ps, it holds that: A = 1, B = 1, and C=1. Then, at t = 0 ps, A becomes 0, and at t = 14 ps, C becomes 0. What happens to output G?



- **a.** The value of G remains the same.
- **b.** The value of G changes once, after 7 ps.
- **c.** The value of G changes once, after 14 ps.
- **d.** A glitch occurs on G (0-1-0 or 1-0-1).

Question 6

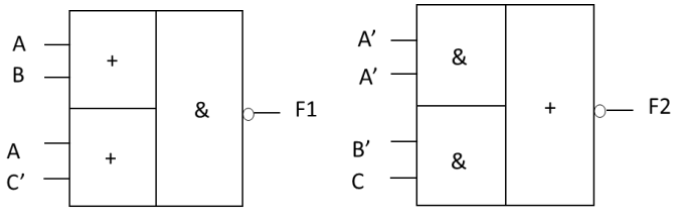
Given the circuit in the figure of Question 5. Which of the following circuits is an equivalent circuit to compute G?

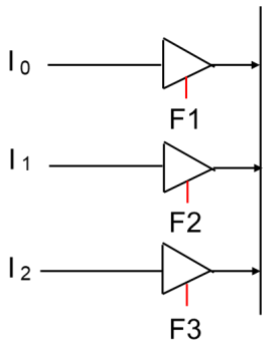


Question 7

Three arbitrary signals are connected to a bus line via Tri-state buffers, as depicted in the figure on the right. Two control functions are specified: F1 and F2, as provided in the figures below. Which third control function F3 can be used such that the circuit operates correctly?

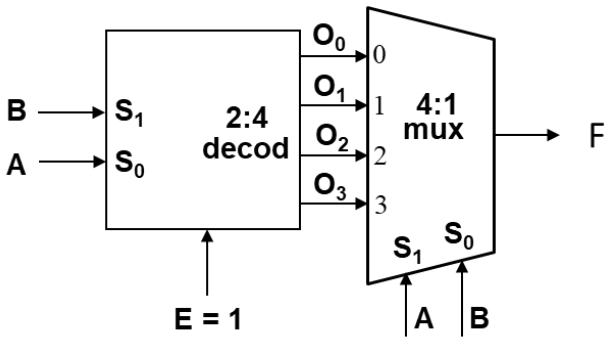
- **a.** F3 = A B C
- **b.** F3 = A B' C
- **c.** F3 = A' B' C'
- **d.** F3 = A' B





Question 8

Given the adjacent circuit. The output F depends on inputs A and B. What is the logic function that describes F in terms of input A and input B.



a. F = A AND B
b. F = A XOR B
c. F = A XNOR B
d. F = 1

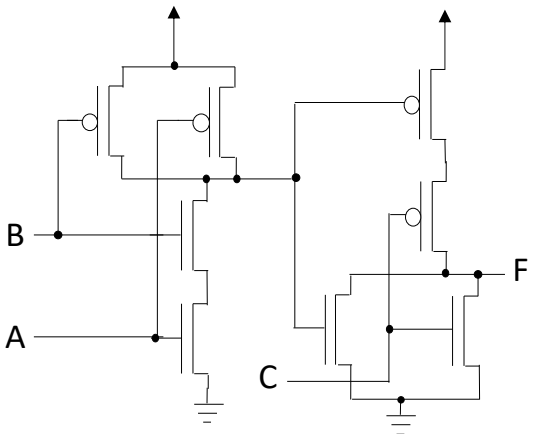
Question 9

Given the following logic NOR/NOR function:
Z = ((A' + B + C)' + (A + B' + C)' + (A' + B' + C)' + (A + B' + C')')'.
What is the minimum number of 2- or 3-input NOR gates that are needed to implement this function. You can assume all inputs and its complementary values are available. You can only use NOR gates.

a. 1 **b.** 2 **c.** 3 **d.** 4

Question 10

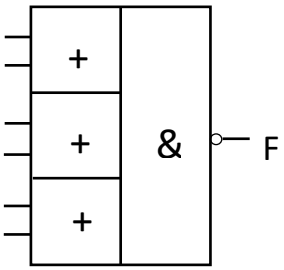
Given the CMOS circuit at the right. Which logical function F is implemented by this circuit?



a. F = A B C'
b. F = A B + C'
c. F = A' + B' + C
d. F = A + B + C'

Question 11

Given the logic expression F = A B + A C + A' C' + B C.
We want to implement this expression with an OR-AND-INVERT gate as depicted at the right. What should we offer to the 3 x 2 inputs of the gate to realize this expression?



a. (A', B'), (A, C) and (A', C')
b. (A, B'), (A, C) and (A', C')
c. (A', C), (A, C) and (B', C)
d. (A', C'), (A, C) and (B', 0)

Question 12

Given the following SystemVerilog statement.

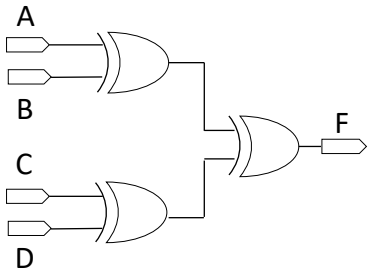
```
assign a = 8'hCD;
```

Which statement will have an equivalent result?

a. `assign a = 8'b10111100;`
b. `assign a = 8'd133;`
c. `assign a = 8'o315;`
d. None of the above answers is correct.

Question 13

What is a canonical expression for the adjacent circuit?



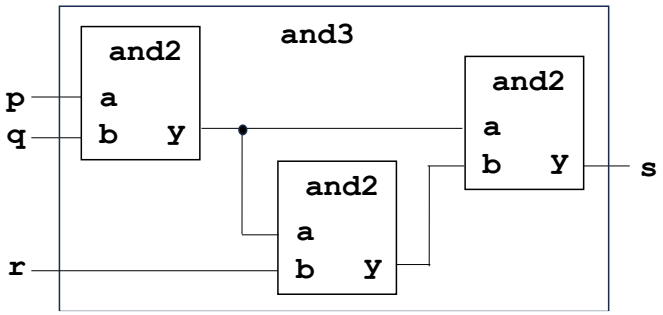
- **a.** F(A,B,C,D) = Π M (0,2,4,6,8,10,12,14)
- **b.** F(A,B,C,D) = Π M (0,3,5,6,9,10,12,15)
- **c.** F(A,B,C,D) = Π M (1,3,5,7,9,11,13,15)
- **d.** F(A,B,C,D) = Π M (1,2,4,7,8,11,13,14)

Question 14

Given the following SystemVerilog description for module **and2**.

```
module and2(input  logic a, b,
            output logic y);
   assign y = a & b;
endmodule
```

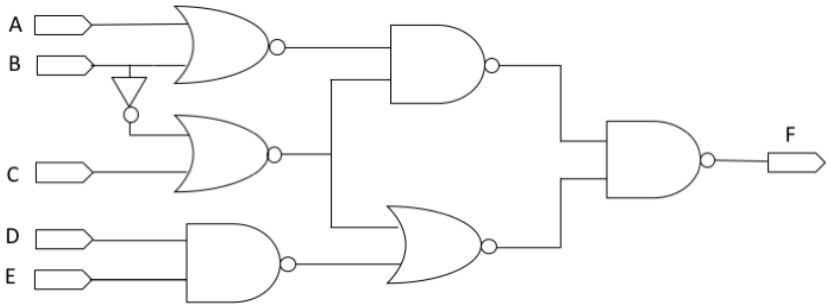
How can the module **and3**, as shown at the right. be implemented in SystemVerilog?




```
a.   module and3 (input logic p, q, r, output logic s);
        and2 i1 (.a(p), .b(q), .y(a));
        and2 i2 (.a(y), .b(c), .y(b));
        and2 i3 (.a(y), .b(y), .y(s));
     endmodule

b.   module and3 (input logic p, q, r, output logic s);
        logic m, n;
        and2 i1 (.a(n), .b(m), .y(s));
        and2 i2 (.a(p), .b(q), .y(n));
        and2 i3 (.a(n), .b(r), .y(m));
     endmodule

c.   module and3 (input logic p, q, r, output logic s);
        logic m, n;
        and2 i1 (p, q, m);
        and2 i2 (n, r, m);
        and2 i3 (n, m, s);
     endmodule

d.   module and3 (input logic p, q, r, output logic s);
        logic m, n;
        and2 i1 (s, n, m);
        and2 i2 (m, p, q);
        and2 i3 (m, n, r);
     endmodule
```

Question 15

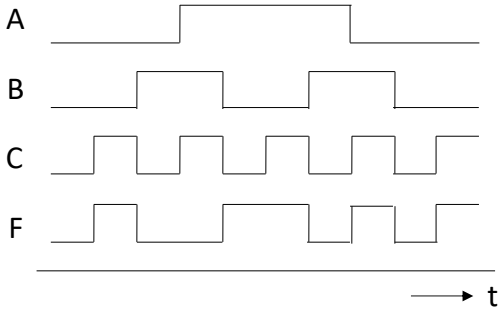
Given the adjacent circuit diagram. What is a logic expression for F?



- **a.** F = B C' + D' + E'
- **b.** F = B' C' + D' + E'
- **c.** F = B + C' + D' E'
- **d.** F = B' + C' + D' E'

Question 16

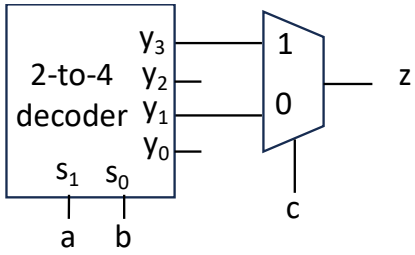
Given the adjacent timing diagram of a circuit with inputs A, B and C, and output F. Which logic function can describe F?



- **a.** F(A,B,C) = A C' + A' C
- **b.** F(A,B,C) = A B' + A C + B' C
- **c.** F(A,B,C) = A C' + A' C + B' C
- **d.** F(A,B,C) = A B' + A' C

Question 17

Given the adjacent circuit with inputs a, b and c, and output z. Which SystemVerilog behavioural statement implements the same logic function?



- **a.** `assign z = ~a & b & ~c | a & b & c;`
- **b.** `assign z = a & ~b & ~c | ~a & ~b & c;`
- **c.** `assign z = c ? ~a & b : a & b;`
- **d.** `assign z = c ? a & ~b : ~a & ~b;`

See next page for Question 18.

Question 18

Given the following SystemVerilog descriptions:

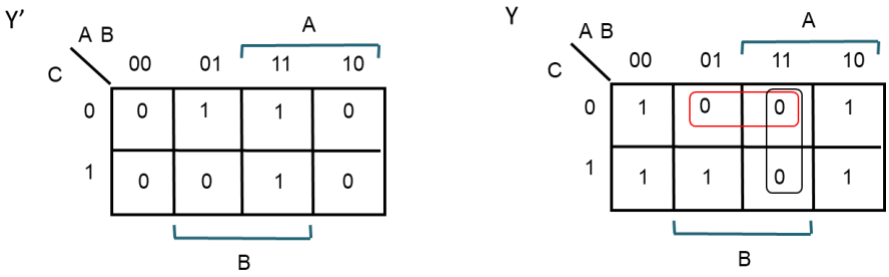
```
module gate1(input  logic a, b,
             output logic y);
   assign #4 y = ~(a ^ b);
endmodule

module gate2(input  logic a, b,
             output logic y);
   assign #3 y = ~(a & b);
endmodule

module mycircuit(input  logic a, b, c,
                 output logic y);
   logic n;
   gate1 i1 (a, n, y);
   gate2 i2 (b, c, n);
endmodule

module mycircuit_tb();
   logic a, b, c, y;

   mycircuit dut(a, b, c, y);

   initial begin
           a = 0; b = 0; c = 0;
      #10; c = 1;
      #10; b = 1;
      #10; a = 1;
   end
endmodule
```

When these descriptions are simulated, at what time will signal y become 1?

a. 7 **b.** 23 **c.** 27 **d.** 34

Answers 1st partial exam EE1D1 4 October 2024

Question 1 b



From the right K-map, it follows that Y = (A' + B') (B' + C)
Or Y = (AB + BC')' = (AB)'(BC')' = (A' + B') (B' + C)

Question 2 c

The number of sum terms (looking at the minimal product-of-sums) equals to one as all zeros can be covered by one rectangle
For the number of product terms (looking at the minimal sum-of-products), two rectangles are required to cover all ones.

Question 3 a

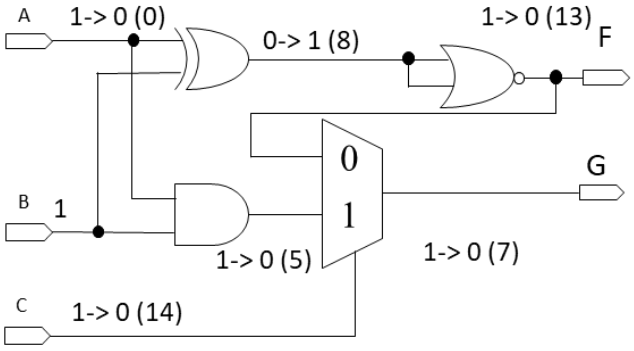
$-25 = -1.5625 * 2^4$ (divide 25 by a power of 2 to find a value between 1 and 2)
$0.5625_{10} = (0.5 + 1/16)_{10} = (2^{-1} + 2^{-4}) = 0.1001_2$

$V = (-1)^s * (1+M) * 2^{E-127}$
S =1, M= 10010000…, $E = (4+127)_{10} = 10000011$

Question 4 d

101011 (-32+8+2+1 = -21)
000101- (5)
100110 (-26)

Question 5 b



Question 6 a

G = C A B + **C' (A ⊕ B)'** = C A B + C' (A' B + A B')' = C A B + C' (A' B)' (A B')'
= C A B + C' (A+B') (A' + B) = C A B + **C'AB + C'A'B'** = B (A) + B' (A' C')

Question 7 b

F1′

C \ A B	00	01	11	10
0	0	1	1	1
1	0	0	1	1

B

F2′

C \ A B	00	01	11	10
0	1	1	0	0
1	1	1	0	1

B

F1+F2

C \ A B	00	01	11	10
0	F1	-	F2	F2
1	F1	F1	**F2**	-

B

F3 can take any terms where there is a -, hence AB'C and/or A' BC'

Question 8 c

O0 = B' A'
O1 = B' A
O2 = B A'
O3 = B A
F = A'B' O0 + A'B O1 + AB'O2 + AB O3 = A'B' + AB = A XNOR B

Question 9 c

Z = ((A' + B + C)' + (A + B' + C)' + (A' + B' + C)' + (A + B' + C')')'
(A' + B + C) (A + B' + C) (A' + B' + C) (A + B' + C') = > K-map

Y′

C \ A B	00	01	11	10
0	1	0	0	0
1	1	0	1	1

B

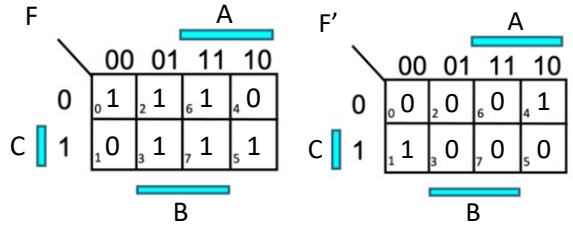
The minimum product of sums equals: (A + B')(A' + C) =>
(A + B')(A' + C) = ((A + B')' + (A' + C)')' => 3 NOR gates

Question 10 a

The left part implements a NAND: E = (A B)'
The right part implements a NOR: F = (E + C)'
Combining them yields: F = ((A B)' + C)' = A B C'

Question 11 d

F = A B + A C + A' C' + B C



Hence F'= (A' + C')(A + C)(B') = (A' + C')(A + C)(B' + 0)

Question 12 c

`8'hCD` is 12 x 16 + 13 = 192 + 13 = 205 in decimal notation,
which is 315 (= 3 x 64 + 1 x 8 + 5) in octal notation.

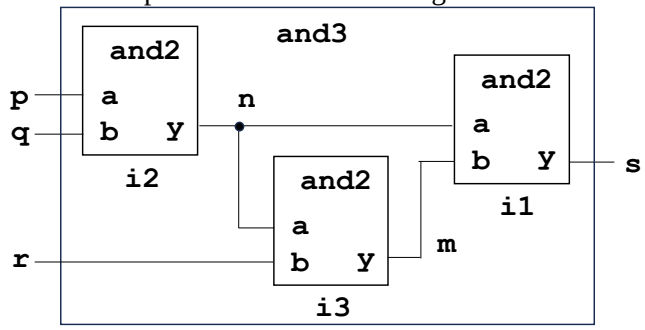
Question 13 b

A	B	C	D	F	
0	0	0	0	0	M_0
0	0	0	1	1	
0	0	1	0	1	
0	0	1	1	0	M_3
0	1	0	0	1	
0	1	0	1	0	M_5
0	1	1	0	0	M_6
0	1	1	1	1	
1	0	0	0	1	
1	0	0	1	0	M_9
1	0	1	0	0	M_{10}
1	0	1	1	1	
1	1	0	0	0	M_{12}
1	1	0	1	1	
1	1	1	0	1	
1	1	1	1	0	M_{15}

The circuit provides a 0 if, and only if, there is an even number of 1's in the input.

Question 14 b

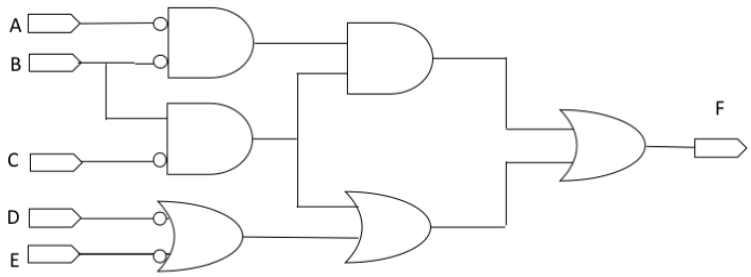
With answer a, there are no local nodes declared and e.g. the output of i1, which has both inputs connected to input ports p and q, does not connect to an input of i2 or i3.
Answer b implements the circuit using instance names and local signals as shown below



With answer c, the output of the and2 that has inputs p and q (i1) does not connect to an input of both other and modules (i2 and i3).
With answer d, there is, among other things, no and2 that has s as output.

Question 15 a

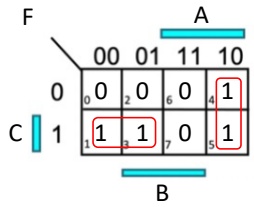
Converting some NORs into ANDs with inverted inputs and some NANDs into ORs with inverted inputs yields the circuit below.



((A' B') (B C')) + ((B C') + (D' + E'))
= B C' + D' + E'

Question 16 d

From the timing diagram we can derive the following K-map and logical function for F:



F = A B' + A' C

Question 17 a

From the decoder it follows:

```
y3 = a & b;
y1 = ~a & b;
```

From the multiplexer it follows: `z = c ? y3 : y1` or `z = y3 c | y1 ~c;`

So

```
assign z = ~a & b & ~c | a & b & c;
```

Answer a connects the AND to the 0 input of the multiplexer and c to the 1 input.
Answer c implements an OR on the 1 input of the multiplexer.
Answer d has the same problem as answer a.

Question 18 c

The module mycircuit is shown at the right, including the signal values after the first stabilization. Below a simulation result is shown.