Trial/Mock Exam Digital Systems A (EE1D1)
24 September 2024, 11.45 – 12.45 h

This exam is an **open book** exam. During the exam you may use: the course book (or any other book about the topic, also prints of books are allowed), the lecture slides, and the lab manual. NOT allowed are the instruction slides, old tests and exams, notes, and electronic equipment - other than a simple, non-programmable, calculator. If you do not adhere to this, the exam fraud rules apply.

The exam consists of 4 pages and contains **10 multiple choice (MC) questions**, each with equal weight. The MC questions must be answered on the issued MC form. Some instructions when filling in the MC form:

- Only one answer is the correct answer.
- Draw a cross on the bubble with letter of your choice (preferably with ballpoint pen, or with pencil), as shown in the example on the MC form.
- Only fill in the form at the end of the exam to avoid mistakes.
- Leaving a question unanswered always works to your disadvantage.
- Do not forget to fill out your name and student number (digits and bubbles!).

This trial/mock exam is also the first of 2 tests that may provide you a bonus for your final grade.

Good luck!

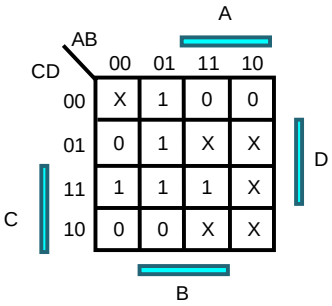
Question 1

What is a simplification for the following logical expression: Y = (A' + B')' + (A + B') C' + B C ?

a. Y = A' B' + A C' + B C
b. Y = A B + B C + B' C'
c. Y = A B + A C' + B C
d. Y = A' B' + B C + B' C'

Question 2

Give a minimal product of sums for the K-map below (X means "don't care").



a. F = (A' + B) (A' + C) (C' + D)
b. F = (A' + C) (B + D') (C' + D)
c. F = (A' + C) (B + D) (C' + D)
d. F = (A' + D) (B + C) (C' + D)

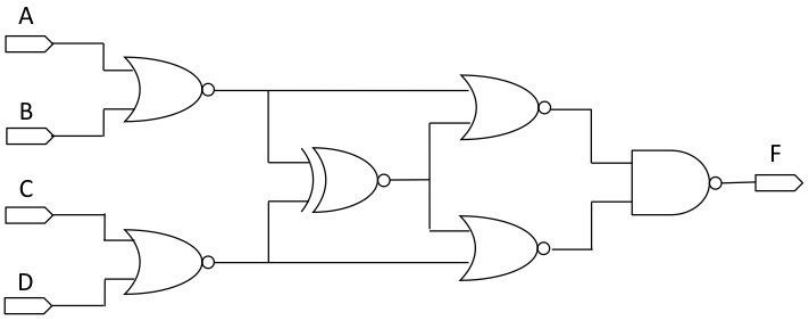
Question 3

What is the 6 bits two's complement notation for the decimal value -14?

a. 101110 **b.** 110001 **c.** 110010 **d.** 110011

Question 4

Given the circuit on the right. The delay time for a NAND gate is 5 ps, for a NOR gate 4 ps, and for an EXNOR gate 12 ps. Initially, just before t = 0 ps, it holds that: A = 0, B = 0, C = 0 and D = 1. Then, at t = 0 ps, A becomes 1. What happens to output F?

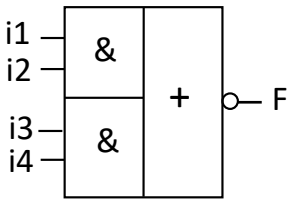


- **a.** F goes from 1 to 0 after 25 ps and doesn't change after that.
- **b.** F goes from 1 to 0 after 13 ps and doesn't change after that.
- **c.** A 1-0-1 glitch occurs at F.
- **d.** F stays 1.

Question 5

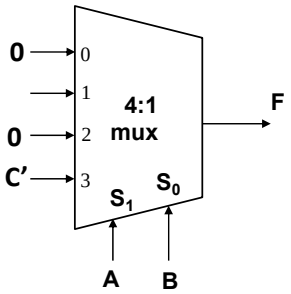
Given the logical expression F = A' B + A C'. Which signals (i1, i2) and (i3, i4) should be offered to the inputs of the following AND-OR-INVERT gate in order to implement this logical function?

- **a.** (A' B') and (A C)
- **b.** (A' B) and (A C')
- **c.** (A B') and (A' C')
- **d.** (A B) and (A' C)



Question 6

Given the following multiplexer circuit. What should be offered on input 1 to ensure that the circuit implements the following logical function: F = A' B C + B C'.



- **a.** 0
- **b.** 1
- **c.** C
- **d.** C'

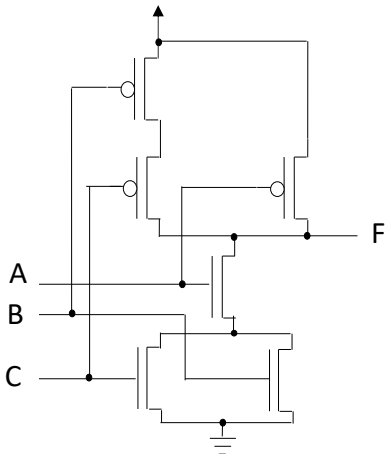
Question 7

Given the logical function F(A, B, C) = A B + B' C. What is the correct canonical form?

- **a.** F(A, B, C) = ∏ M(3, 4, 5, 7)
- **b.** F(A, B, C) = ∏ M(0, 1, 2, 6)
- **c.** F(A, B, C) = ∏ M(1, 5, 6, 7)
- **d.** F(A, B, C) = ∏ M(0, 2, 3, 4)

Question 8

Given the CMOS circuit at the right. Which logical function F is implemented by this circuit?



- **a.** F = A' + (B + C)'
- **b.** F = A' (B + C)
- **c.** F = A' (B + C)'
- **d.** F = A' + (B C)'

Question 9

Given the following description of a SystemVerilog module and testbench:

```
module func1(input  logic a, b, c,
             output logic y);
   logic n1, n2;

   assign #4 y = n2 & n1;
   assign #1 n1 = ~b;
   assign #2 n2 = a | c;
endmodule

module testfunc1();
   logic a, b, c, y;

   func1 dut(a, b, c, y);

   initial begin
          a = 0; b = 1; c = 0;
      #8; a = 1;
      #8; b = 0;
      #8; c = 1;
   end
endmodule
```

When these descriptions are simulated, at what time will signal y go from 0 to 1?

- **a.** 16
- **b.** 20
- **c.** 21
- **d.** 23

Question 10

Given the following logical function F(a,b,c) = Σ m(2, 3, 4, 6)
What is a correct SystemVerilog description that implements this logic function?

a.

```
module circuit (input logic a, b, c, output logic y);
   logic n1, n2;
   assign y = n1 & n2;
   assign n1 = ~a & ~b;
   assign n2 = a | c;
endmodule
```

b.

```
module circuit (input logic a, b, c, output logic y);
   logic n1, n2;
   assign y = n1 | n2;
   assign n1 = ~a & b;
   assign n2 = a & ~c;
endmodule
```

c.

```
module circuit (input logic a, b, c, output logic y);
   assign y = ~a & ~b | a & ~c;
endmodule
```

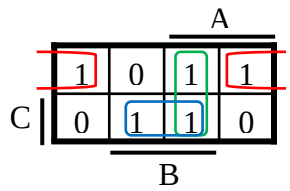
d.

```
module circuit (input logic a, b, c, output logic y);
   assign y = ~a & b | a & c;
endmodule
```

Answers mock exam EE1D1 24 September 2024

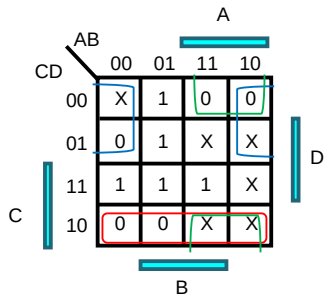
Question 1 b

Y = (A' + B')' + (A + B') C' + B C
= A B + A C' + B' C' + B C



Y = A B + B C + B' C'

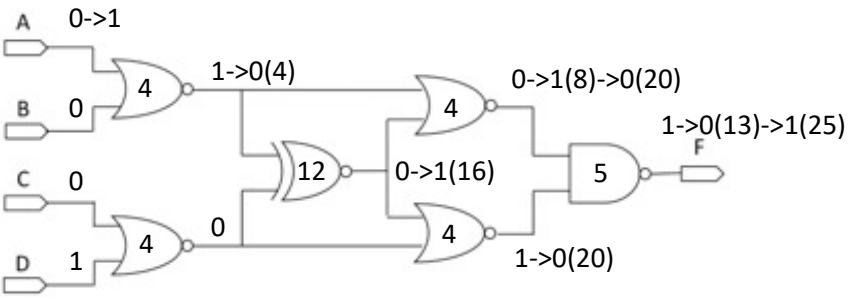
Question 2 d



F = (A' + D) (B + C) (C' + D)

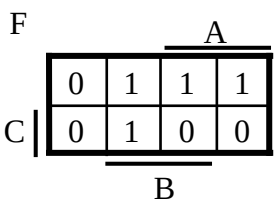
Question 3 c
14 = 001110
-14 = 110001 + 1 = 110010

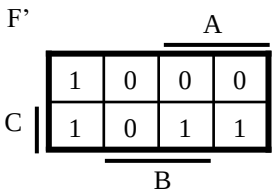
Question 4 c



Question 5 a

A K-map for F is shown on the right.
The AND-OR part of the AOI gate should implement F', which is also shown.
Hence, F' = A' B' + A C.





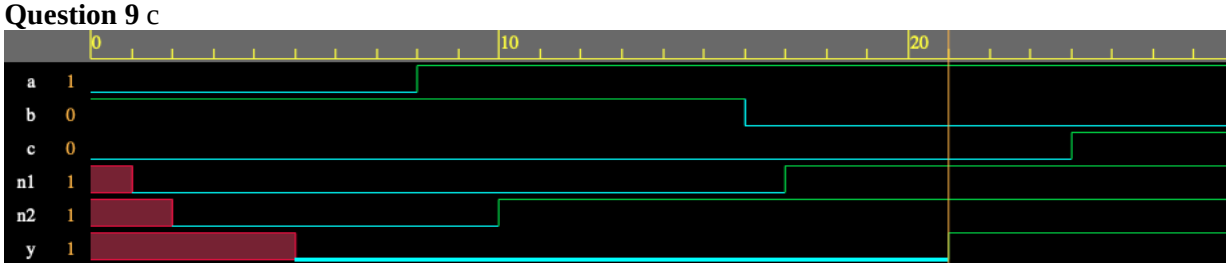
Question 6 b
Input 1 is selected when A=0 and B=1. Then F= 0’ 1 C + 1 C’ = C + C’ = 1

Question 7 d
Make a truth-table for A B + B’ C to see when F=0 and hence find the maxterms.

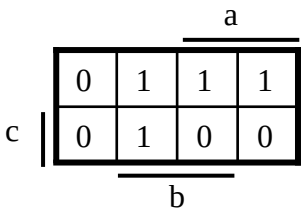
A	B	C	F	
0	0	0	0	M_0
0	0	1	1	
0	1	0	0	M_2
0	1	1	0	M_3
1	0	0	0	M_4
1	0	1	1	
1	1	0	1	
1	1	1	1	

Question 8 a
F is pulled down by the NMOS transistors when A (B + C).
Hence F = (A (B + C))’ = A’ + (B + C)’
Also, F is pulled up by the PMOS transistors when A’ + B’ C’.
This also results in F = A’ + B’ C’ = A’ + (B + C)’, which confirms the answer.

Question 9 c



Question 10 b
Filling out the sum of minterms Σ m(2, 3, 4, 6) in a K-map gives:



An expression that can be derived from it is: F(a,b,c) = a’ b + a c’, which is implemented by answer b.