Mock Exam Digital Systems A (EE1D1)
26 September 2023, 11.45 – 12.30 h

This exam is an **open book** exam. During the exam you may use: the course book (or any other book about the topic, also prints of books are allowed), the lecture slides, and the lab manual. NOT allowed are the instruction slides, old tests and exams notes, and electronic equipment - other than a simple, non-programmable, calculator. If you do not adhere to this, the exam fraud rules apply.

The exam consists of 4 pages and contains **10 multiple choice (MC) questions**, each with equal weight. The MC questions must be answered on the issued MC form. Some instructions when filling in the MC form:

- Only one answer is the correct answer (BTW: a, b, c and d are mixed on the answer sheet).
- Fill in the chosen boxes completely (preferably with ballpoint pen, or with pencil).
- Only fill in the form at the end of the exam to avoid mistakes.
- Do not make any changes: in that case, get a new form
- Leaving a question unanswered always works to your disadvantage.
- Do not forget to enter your student number (numbers and boxes!).

Good luck!

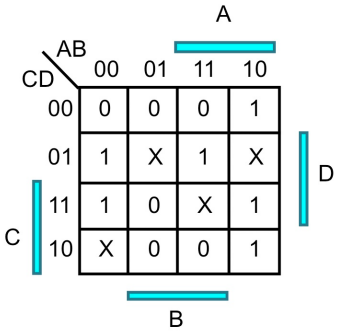
Question 1

What is a simplification for the following logic expression: Y = (A + B)' C + (A + B) C' + A' B ?

a. Y = A C' + A' C + B C'
b. Y = A C' + A' C + B C
c. Y = A C' + A' B + B C'
d. Y = A C' + A' B + B C

Question 2

Give a minimal sum of products for the K-map below (X means "don't care").



a. F = A B' + A D + C' D
b. F = B' C + B' D + C' D
c. F = A D + B' D + C' D
d. F = A B' + B' C + C' D

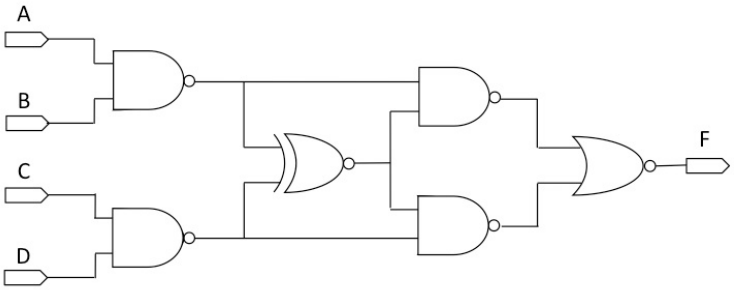
Question 3

Given the 6 bits two's complement notation 110110. What is the decimal value?

a. -22 **b.** -10 **c.** -9 **d.** -8

Question 4

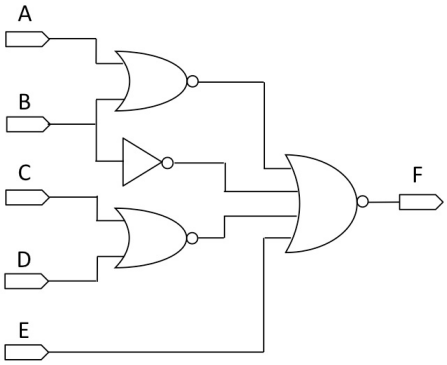
Given the circuit at the right. The delay time for a NAND gate is 5 ps, for a NOR gate 4 ps, and for an EXNOR gate 12 ps. Initially, just before t = 0 ps, it holds that: A = 0, B = 1, C = 0 and D = 1. Then, at t = 0 ps, A becomes 1. What happens to output F ?



a. F goes from 1 to 0 after 26 ps and doesn't change after that.
b. F goes from 1 to 0 after 14 ps and doesn't change after that.
c. A 1-0-1 glitch occurs at F.
d. F stays 1.

Question 5

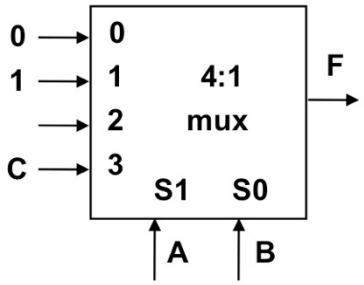
Given the circuit below. What is a logic expression for F ?



a. F = B E' (C + D)
b. F = A E' (C + D)
c. F = B' + C D + E
d. F = A' + C D + E

Question 6

Given the following multiplexer circuit. What should be offered on input 2 to ensure that the circuit implements the following logical function: F = A' B + A C



a. 0
b. 1
c. C
d. C’

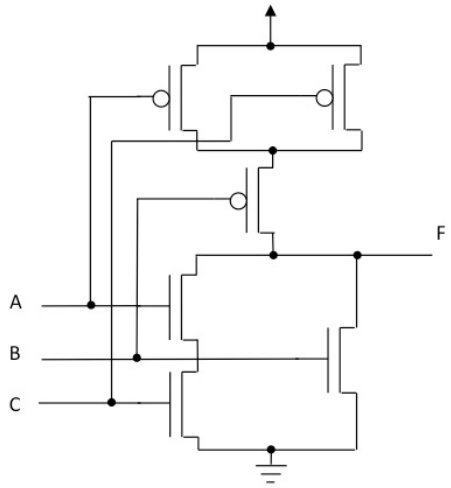
Question 7

Given the logic function F(A, B, C) = A B + C. What is the correct canonical form?

- **a.** F(A, B, C) = Σ m(0, 2, 4)
- **b.** F(A, B, C) = Σ m(0, 2, 4, 6)
- **c.** F(A, B, C) = Σ m(1, 3, 5, 7)
- **d.** F(A, B, C) = Σ m(1, 3, 5, 6, 7)

Question 8

Given the CMOS circuit at the right. Which logical function F is implemented with this circuit?



- **a.** F = (A C + B)'
- **b.** F = A C + B
- **c.** F = (A + C) B
- **d.** F = (A B + B C)'

Question 9

Given the following description of a SystemVerilog module and testbench:

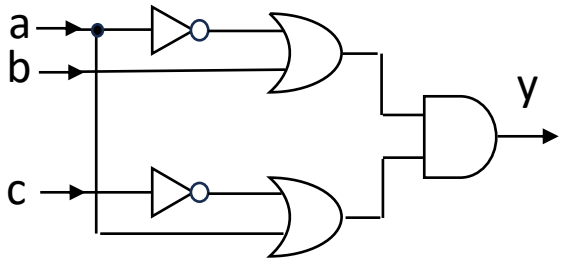
```
module func1(input  logic a, b, c,
             output logic y);
   logic n;

   assign #3 n = b | c;
   assign #2 y = a & n;
endmodule

module testfunc1();
   logic a, b, c, y;

   func1 dut(a, b, c, y);

   initial begin
          a = 0; b = 0; c = 0;
      #6; a = 1;
      #6; b = 1;
      #6; c = 1;
   end
endmodule
```

When these descriptions are simulated, at what time will signal y go from 0 to 1?

- **a.** 12
- **b.** 15
- **c.** 17
- **d.** 18

Question 10

Given the following circuit.



What is a correct SystemVerilog description that implements the same logic function as the following circuit:

a.

```
module circuit (input logic a, b, c, output logic y);
   logic n1, n2;
   assign n1 = a' | b;
   assign n2 = c' | a;
   assign y = n1 & n2;
endmodule
```

b.

```
module circuit (input logic a, b, c, output logic y);
   logic n1, n2;
   assign y = n1 & n2;
   assign n1 = ~a | b;
   assign n2 = ~c | a;
endmodule
```

c.

```
module circuit (input logic a, b, c, output logic y);
   assign y = ~(a | b) & ~(c | a);
endmodule
```

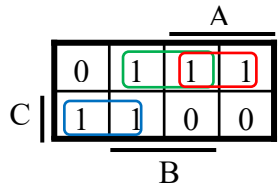
d.

```
module circuit (input logic a, b, c, output logic y);
   assign y = a' | b & c' | a;
endmodule
```

Answers mock exam EE1D1 26 September 2023

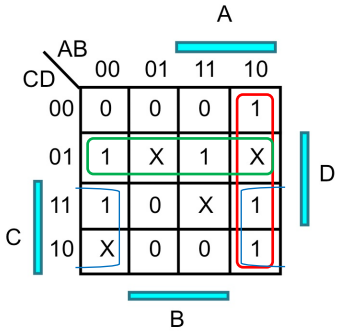
Question 1 a

Y = (A + B)' C + (A + B) C' + A' B
  = A' B' C + A C' + B C' + A' B



Y = A C' + A' C + B C'

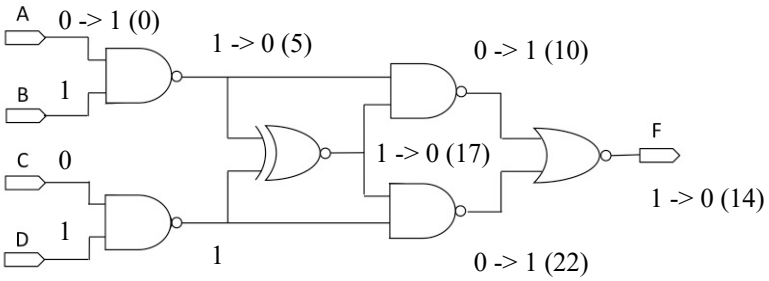
Question 2 d



F = A B' + B' C + C' D

Question 3 b
Since left-most bit is 1, it represents a negative value. Invert all bits and add 1 to find the magnitude:
110110 => 001001 => 001001 + 1 = 001010 => -10

Question 4 b



Question 5 a
The NOR gate with 4 inputs can be converted into a NAND with 4 inverted inputs (DeMorgan).
Then 3 of the inverted inputs cancel against the inversions of the NORs and the INVERTER, and we find the following expression:
F = (A + B) B (C + D) E'
  = (AB + B) (C + D) E'
  = B (C + D) E'

Question 6 c
Input 2 is selected when A=1 and B=0. Then F= 1' 0 + 1 C = C

Question 7 d
Make a truth-table to see when F=1 and hence find the minterms.

A	B	C	F	
0	0	0		
0	0	1	1	m_1
0	1	0		
0	1	1	1	m_3
1	0	0		
1	0	1	1	m_5
1	1	0	1	m_6
1	1	1	1	m_7

Question 8 a
F is pulled down by NMOS transistor when A C + B. Hence F' = (A C + B) or F = (A C + B)'

Question 9 c
At t=12, both a and b have become 1. Then y becomes 1 3+2 = 5 time units later, which is at t=17.

Question 10 b
Answer a and d use quotes for inversion, which is no correct SystemVerilog. Answer c is an AND operation on 2 NOR operations, which is also not correct.